

Fig. 1

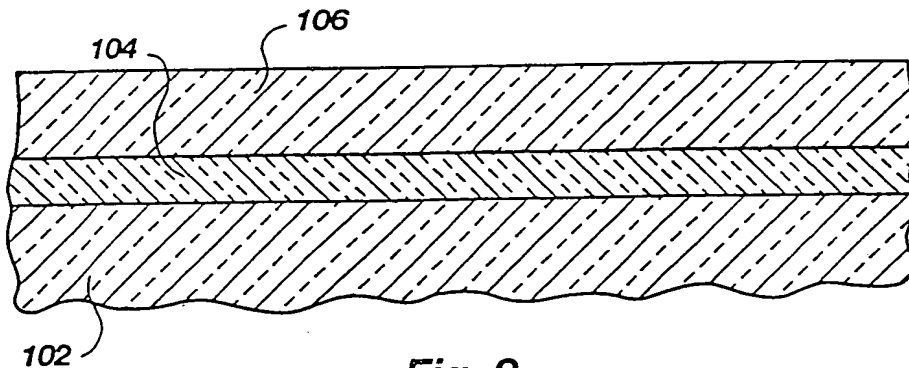


Fig. 2

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETCH

Inventor: Pan et al.
Serial No.: 09/073,494
Docket No.: 2269-2915.1US

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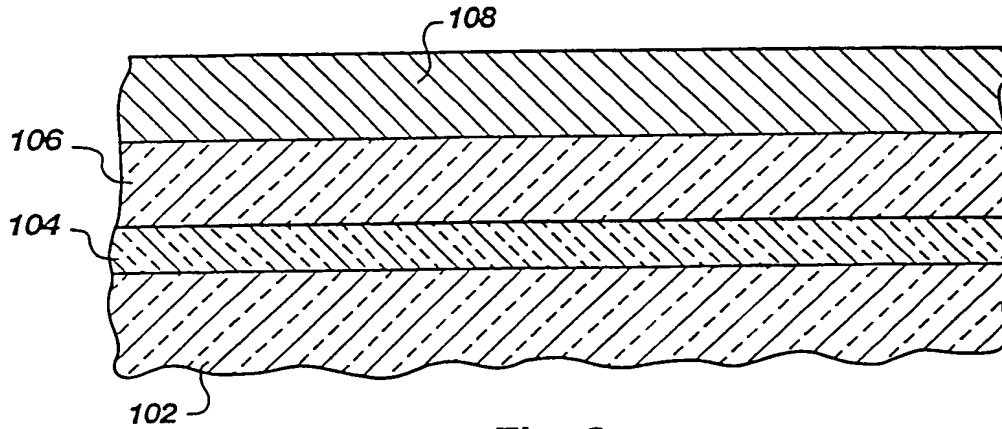
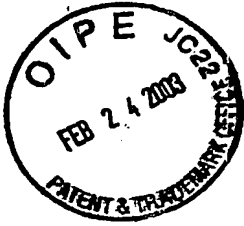


Fig. 3

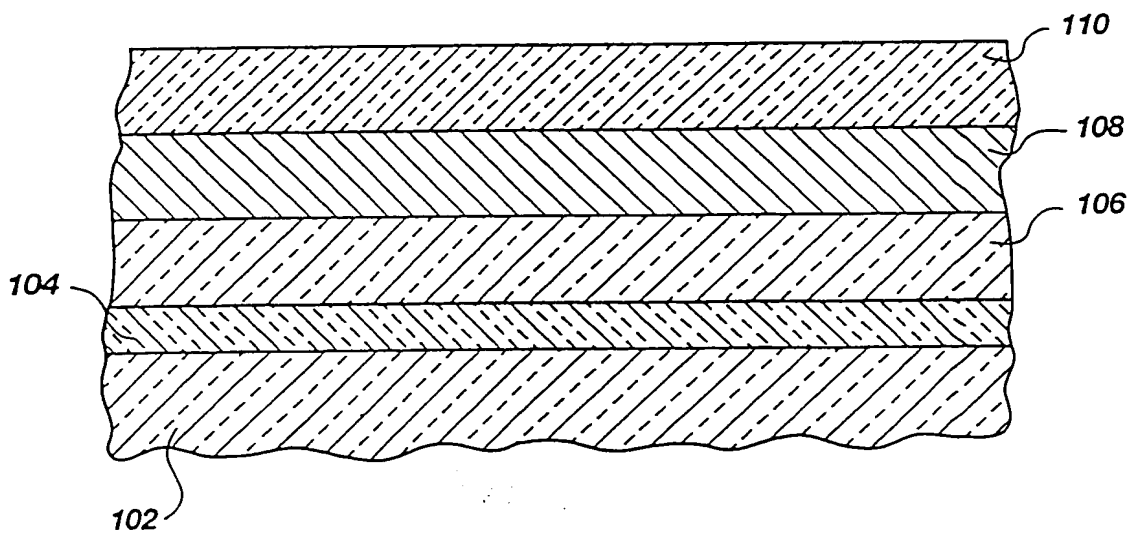


Fig. 4



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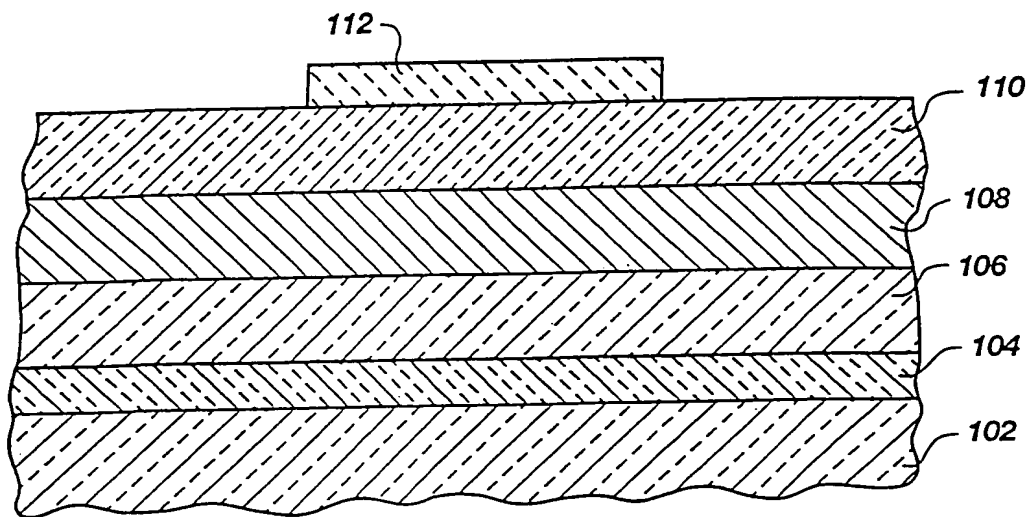


Fig. 5

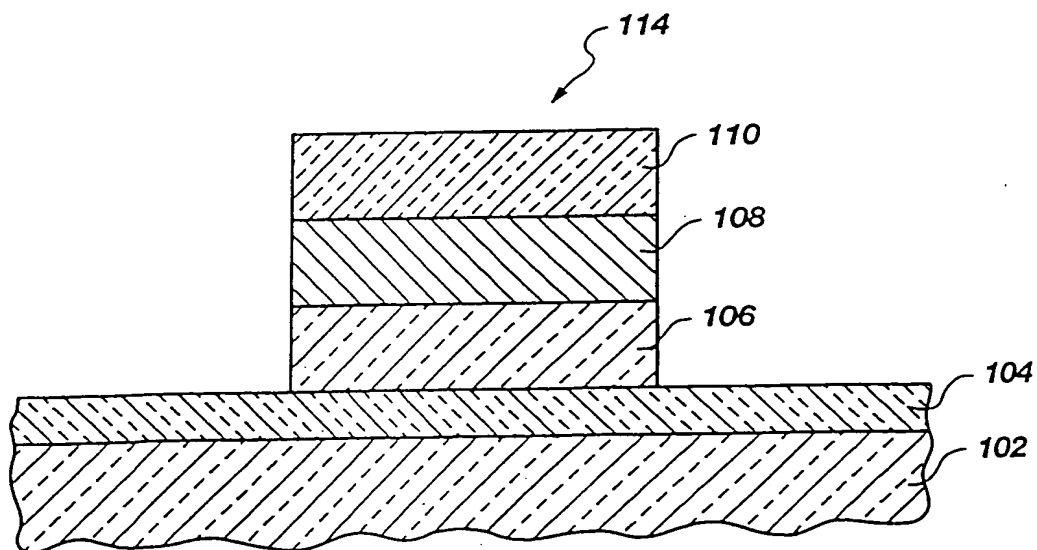


Fig. 6



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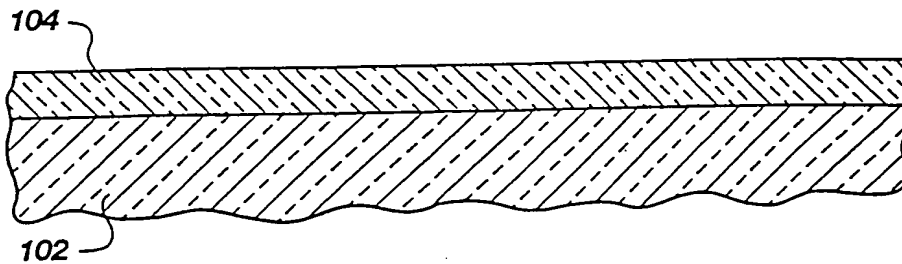


Fig. 7

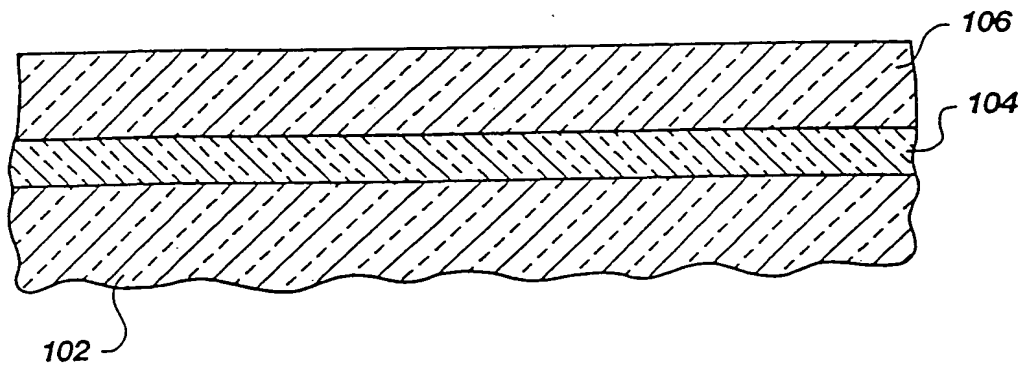
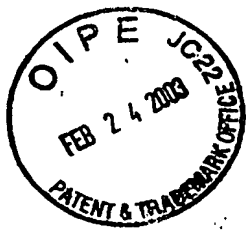


Fig. 8



TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
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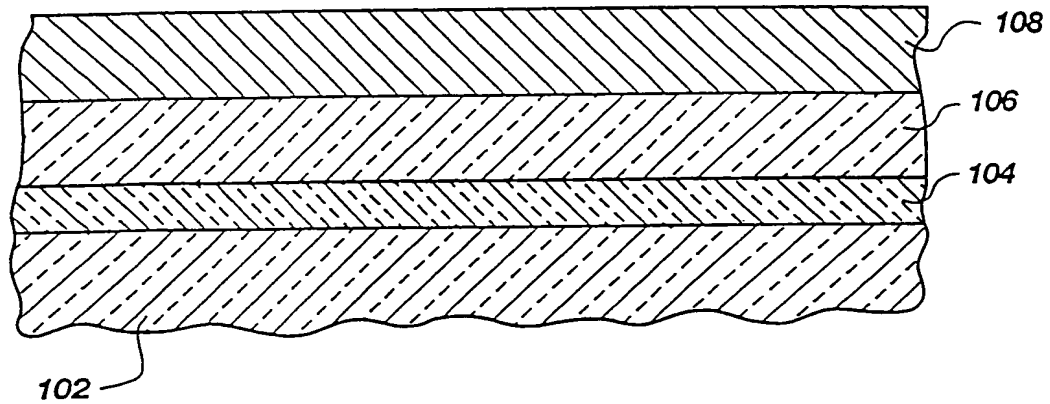


Fig. 9

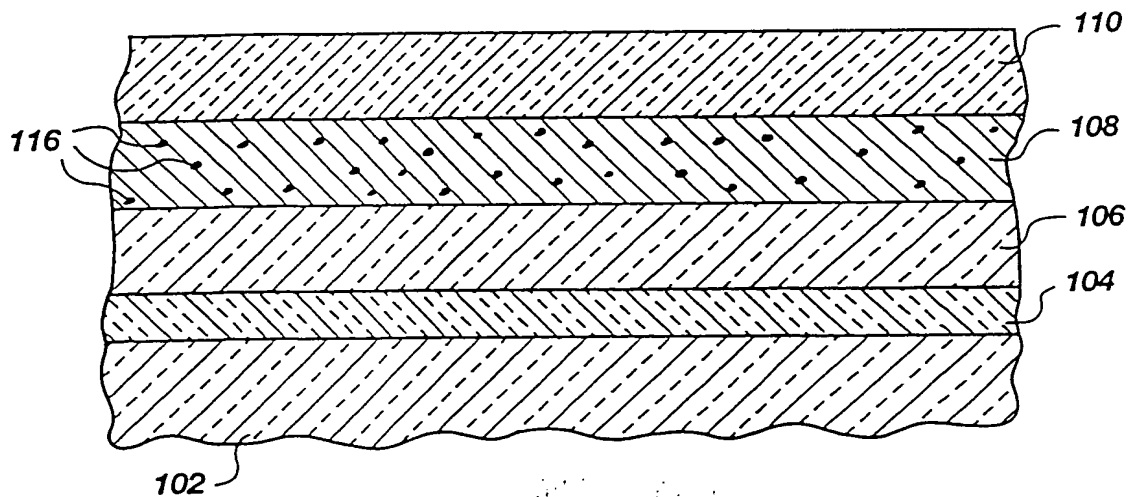
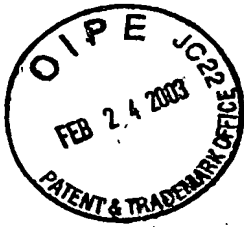


Fig. 10



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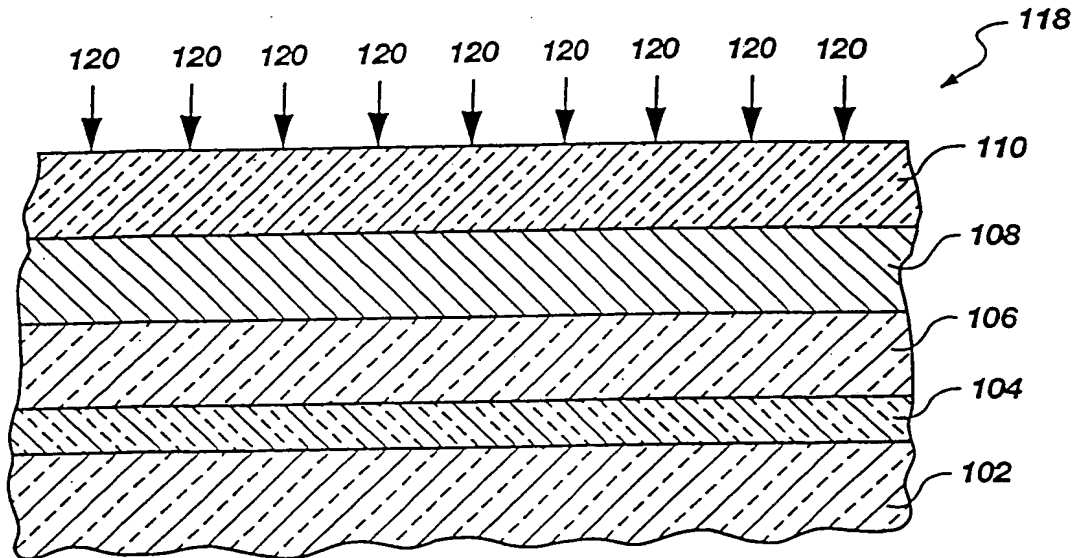


Fig. 11

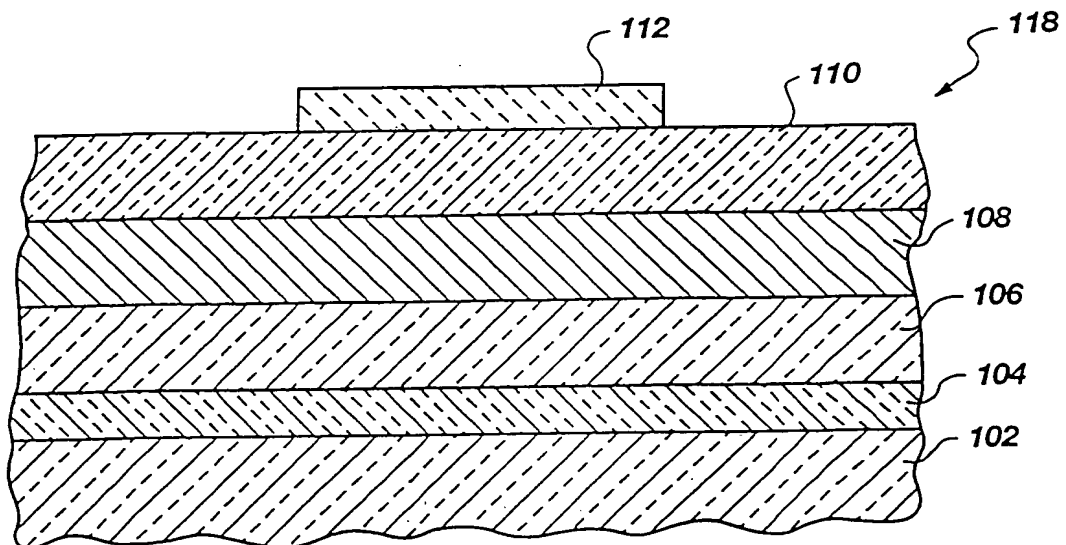


Fig. 12

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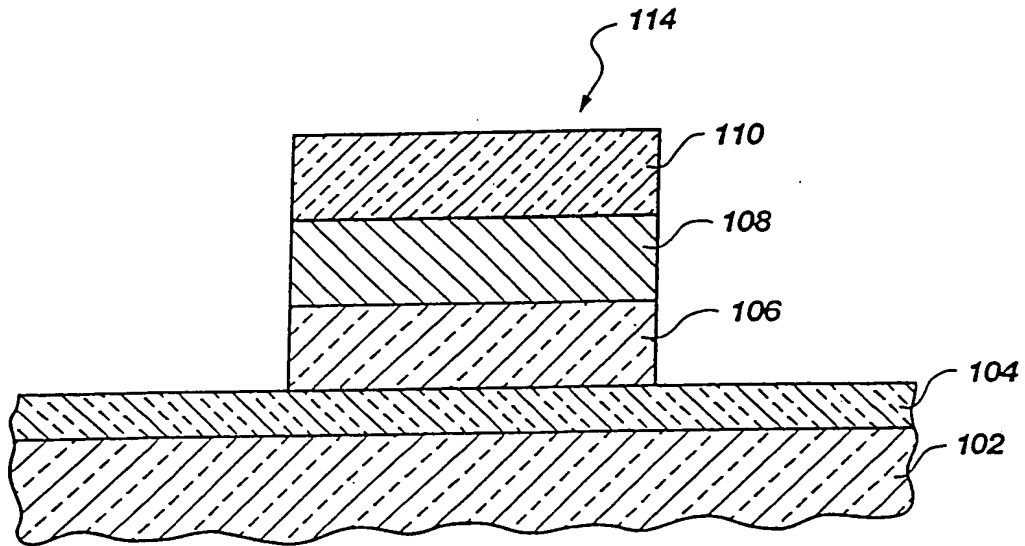


Fig. 13

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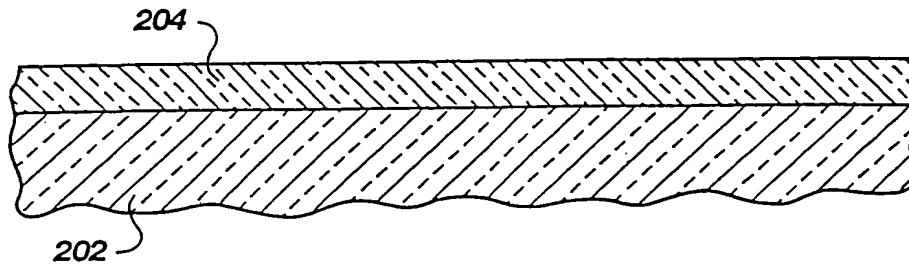
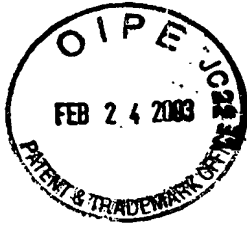


Fig. 14
(PRIOR ART)

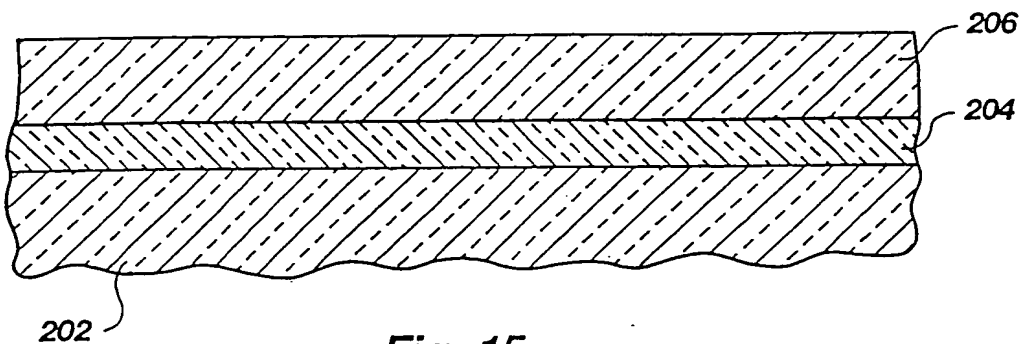


Fig. 15
(PRIOR ART)

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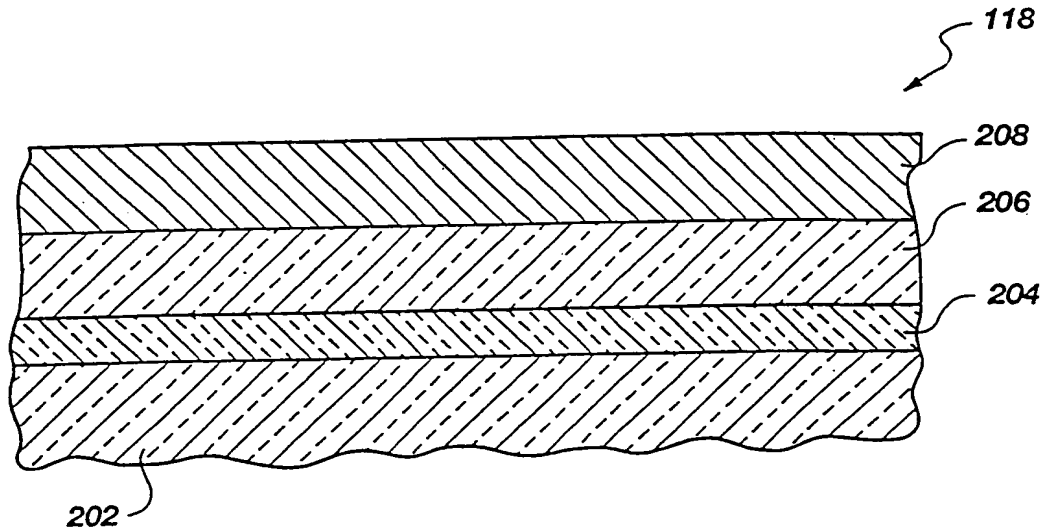


Fig. 16
(PRIOR ART)

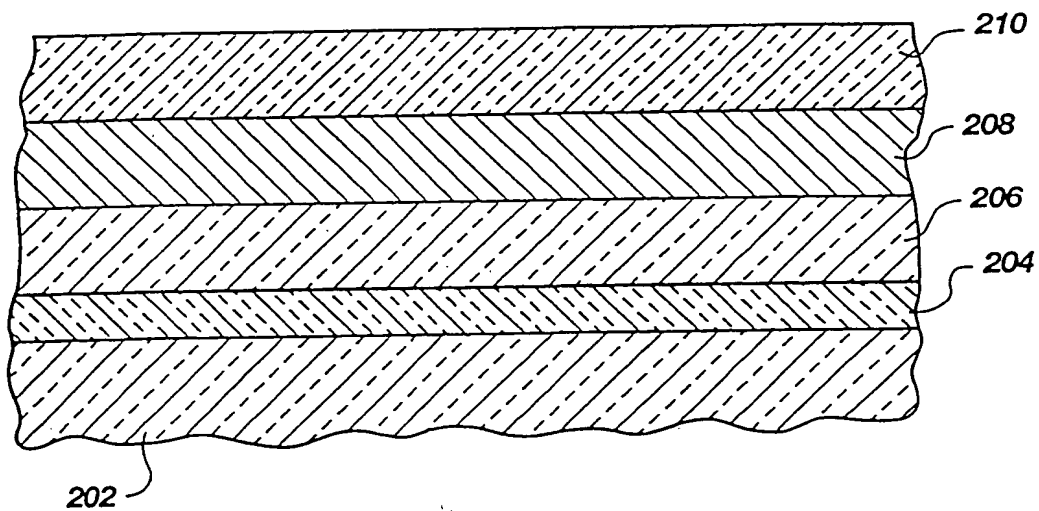


Fig. 17
(PRIOR ART)

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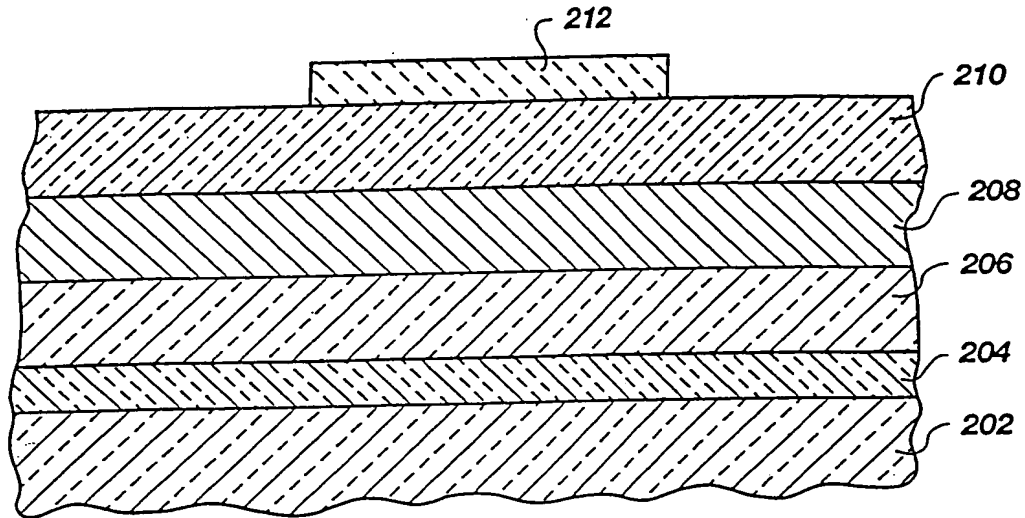


Fig. 18
(PRIOR ART)

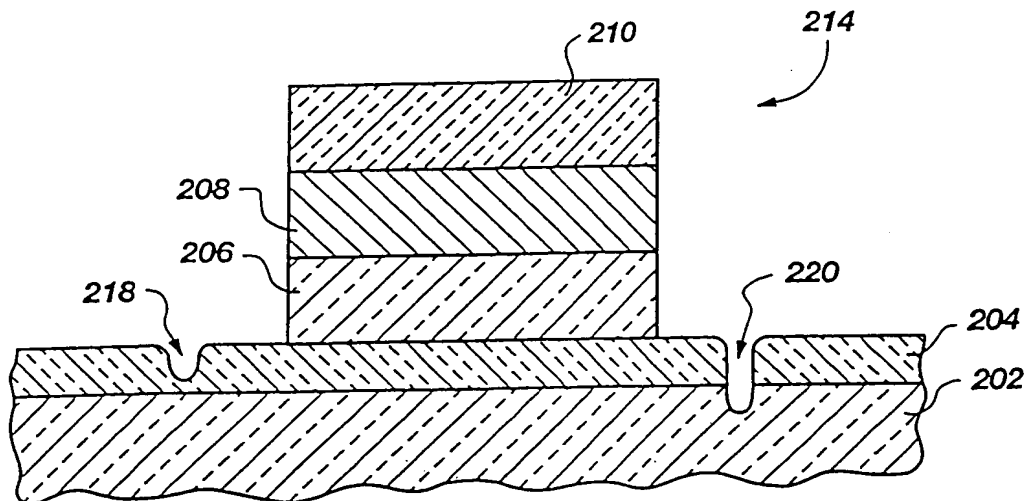


Fig. 19
(PRIOR ART)

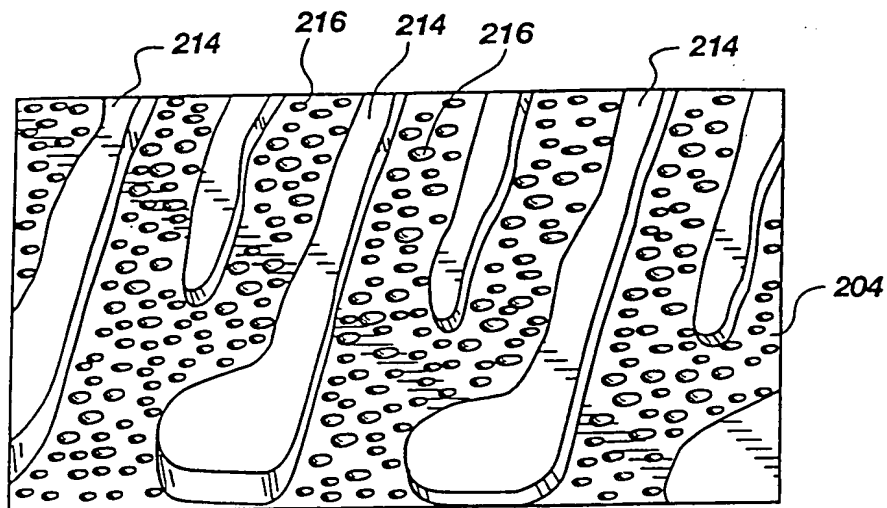


Fig. 20
(PRIOR ART)

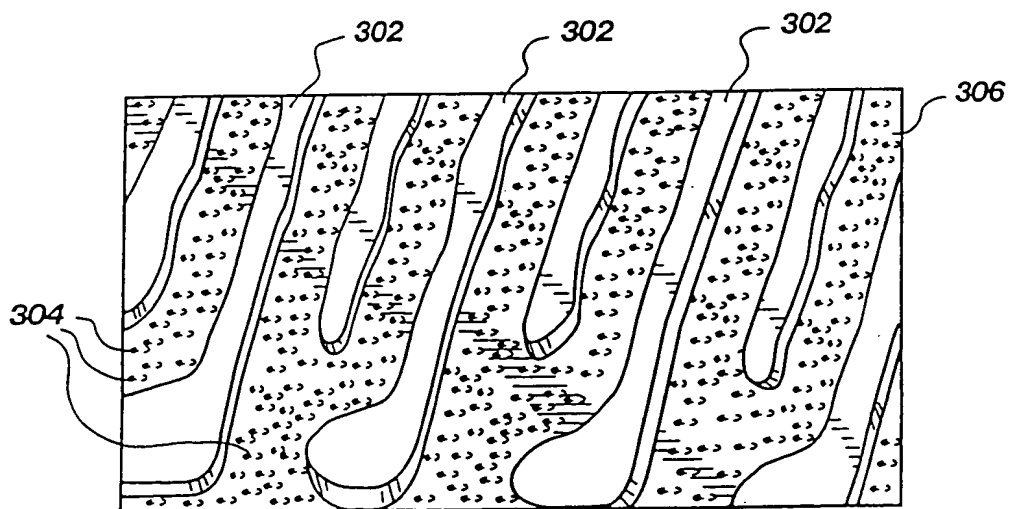


Fig. 21
(PRIOR ART)

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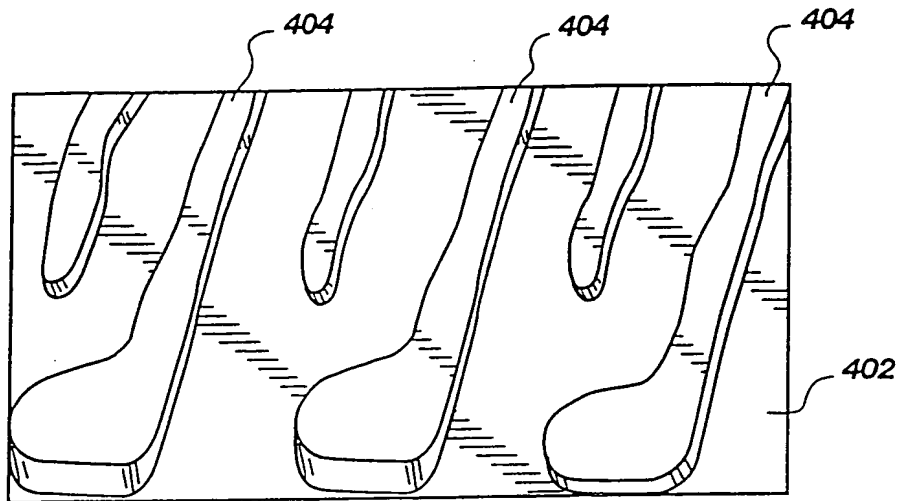


Fig. 22

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETCH

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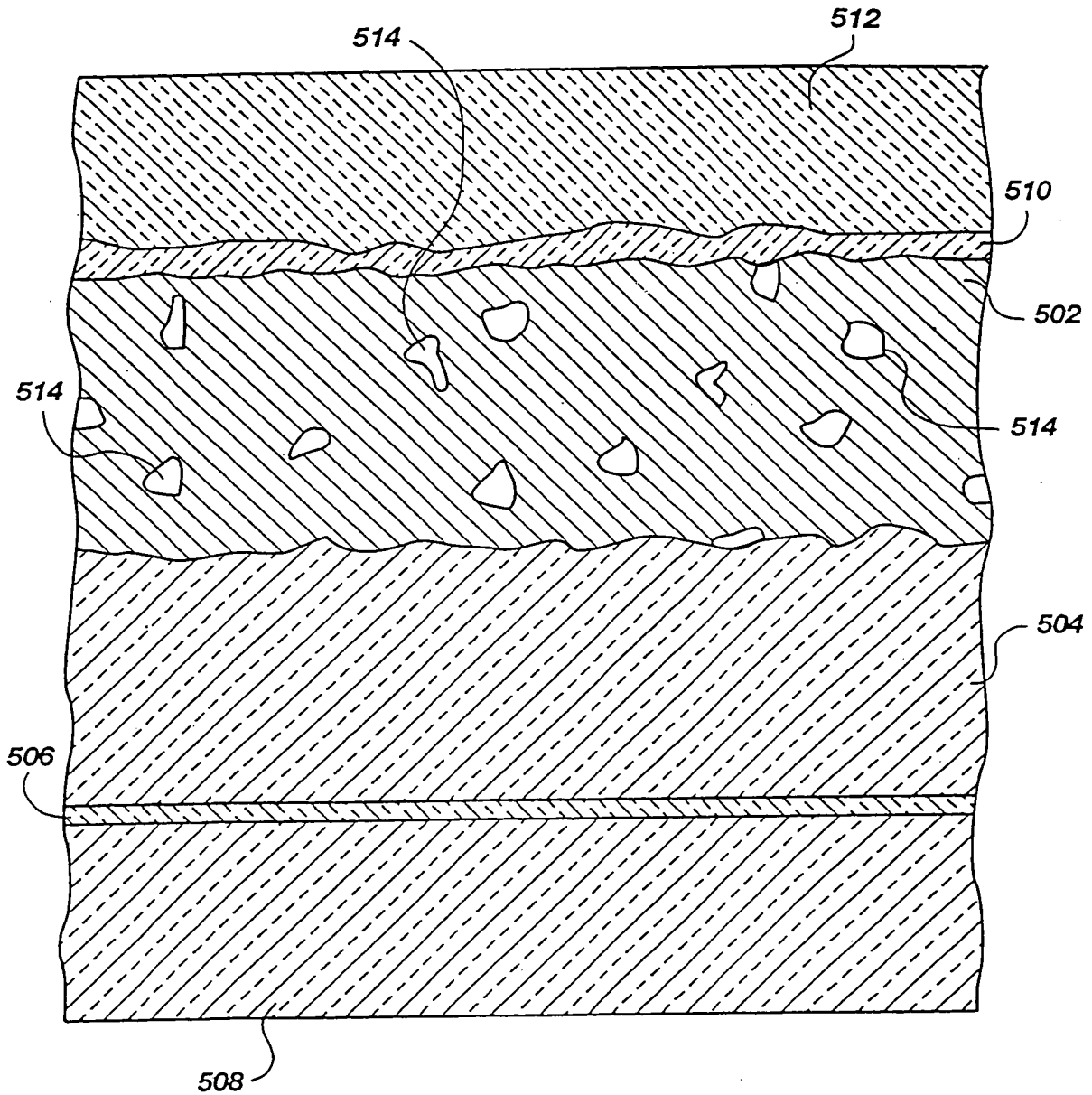


Fig. 23
(PRIOR ART)



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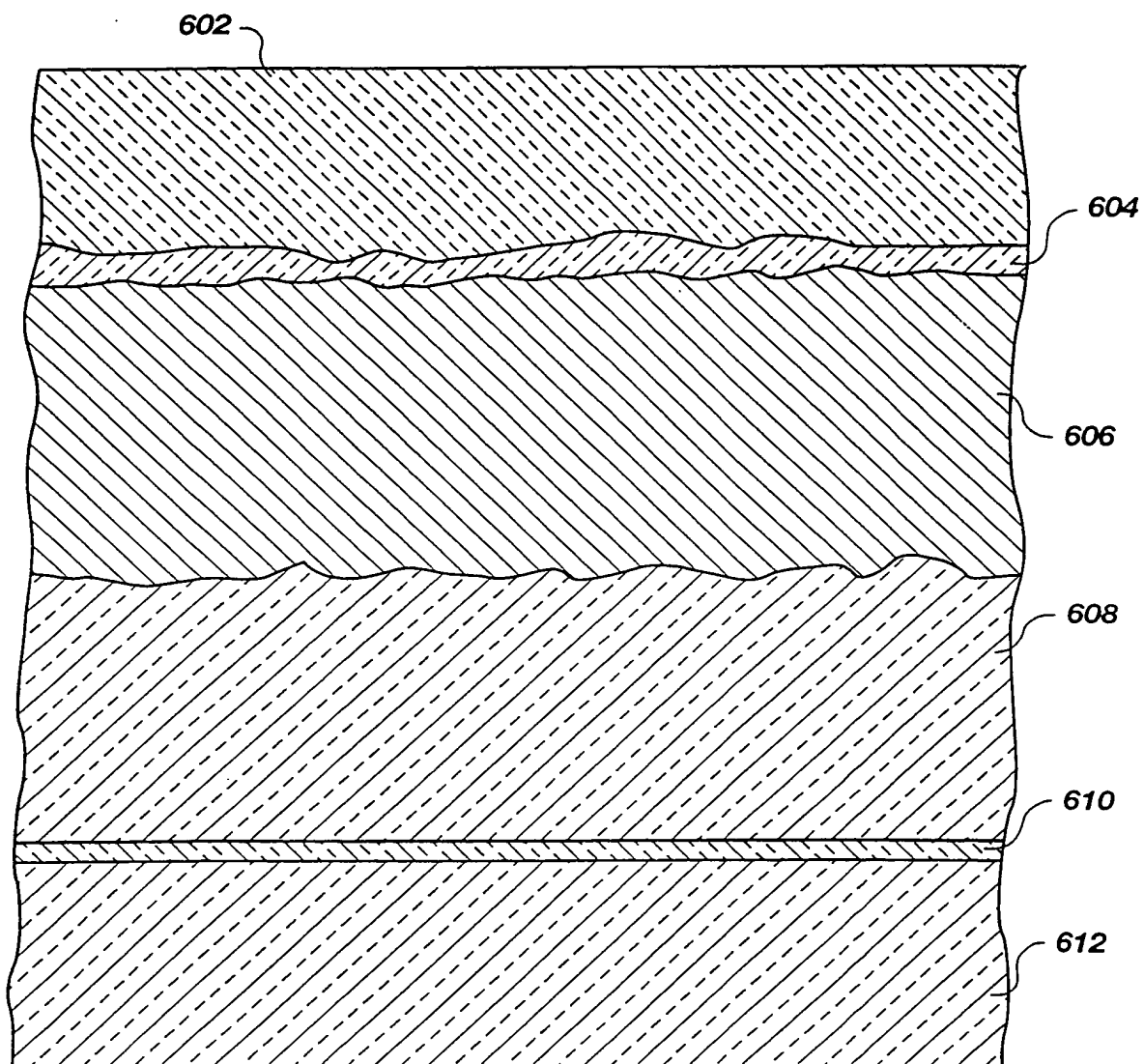


Fig. 24